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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/582,351	08/11/2000	TOSHIYUKI NAKAYAMA	106386	3351
25944	7590	06/14/2004	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			CHU, CHRIS C	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 06/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary**Application No.**

09/582,351

Applicant(s)

NAKAYAMA, TOSHIYUKI

Examiner

Chris C. Chu

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 May 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 10, 12 - 19, 21 and 22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 10, 12 - 19, 21 and 22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Supplemental final rejection

1. In response to applicant's arguments filed on May 28, 2004, this is supplemental Office action correcting an erroneous statement made in the previous Office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6 – 8, 10, 12, 14 – 17, 19, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida et al. '009.

Regarding claim 1, Yoshida et al. discloses in e.g., Fig. 5, Fig. 7D and column 6, lines 26 – 36 a method of manufacture of a semiconductor device (the structure in Fig. 1) comprising the steps of:

- providing an adhesive (22) between a surface of a semiconductor chip (1) having a plurality of electrodes (2) on which said electrodes are provided and a surface of a substrate having a plurality of leads (17) and an undivided film (18) on which said leads and said undivided film are formed;

- positioning at least one of said plurality of electrodes to be opposed to at least one of said plurality of leads such that said undivided film is opposed to said semiconductor chip; and
- applying pressure in a direction such as to make a gap between said semiconductor chip and said substrate narrower such that said adhesive extends to be disposed on the whole of said undivided film;
- wherein said undivided film (18) is formed with a lower adhesion to the adhesive (22) than a base material of the substrate (16), and the undivided film is broader than each of the leads at their portions opposed to the electrodes,
- wherein a region on which the adhesive is disposed includes a first region (at the surface area of the element 18) with low adhesion to the adhesive and a second region (at the gap or space between the leads 17 and the element 18) with high adhesion to the adhesive,
- an area of the first region being \geq an area of the second region.

Inherently, Ag or Sn has lower adhesion to any molding material than polyimide to the molding material because it is known in the art that metal has lower adhesion than polyimide.

Regarding claims 6 and 15, Yoshida et al. discloses in e.g., Fig. 5, Fig. 7D and column 6, lines 26 – 36 the electrodes (2) being provided on an extremity of the surface of the semiconductor chip (1); and the undivided film (18) is formed in a region opposing a central part of the surface of the semiconductor chip.

Regarding claims 7 and 16, Yoshida et al. discloses in e.g., Fig. 5, Fig. 7D and column 6, lines 26 – 36 the undivided film (18) being formed to spread two-dimensionally, with at least one opening exposing a surface of the substrate.

Regarding claims 8 and 17, Yoshida et al. discloses in e.g., Fig. 5, Fig. 7D and column 6, lines 26 – 36 the undivided film (18) being formed to project outside a region in which the semiconductor chip is adhered.

Regarding claims 10 and 19, Yoshida et al. discloses in e.g., Fig. 5, Fig. 7D and column 6, lines 26 – 36 the undivided film (18) being formed to avoid at least one of the leads.

Regarding claim 12, Yoshida et al. discloses in e.g., Fig. 5, Fig. 7D and column 6, lines 26 – 36 a semiconductor device (the structure in Fig. 1) comprising:

- a semiconductor chip (1) having a plurality of electrodes (2);
- a substrate (16) on which is formed a plurality of leads (17) and an undivided film (18), said undivided film opposed to said semiconductor chip; and
- an adhesive (22) provided between a surface of the semiconductor chip (1) on which the electrodes (2) are formed and a surface of the substrate (16) on which said leads (17) and said undivided film (18) are formed, to adhere the semiconductor chip and the substrate,
- said adhesive disposed on the whole of said undivided film,
- wherein at least one of the plurality of electrodes (2) and at least one of the plurality of leads (17) are electrically connected; and

- wherein said undivided film (18) is formed with a lower adhesion to the adhesive (22) than a base material of the substrate (16), and the undivided film is broader than each of the leads at their portions opposed to the electrodes,
- wherein a region on which the adhesive is disposed includes a first region (at the surface area of the element 18) with low adhesion to the adhesive and a second region (at the gap or space between the leads 17 and the element 18) with high adhesion to the adhesive,
- an area of the first region being \geq an area of the second region.

Inherently, Ag or Sn has lower adhesion to any molding material than polyimide to the molding material because it is known in the art that metal has lower adhesion than polyimide.

Regarding claim 14, Yoshida et al. discloses in e.g., Fig. 5, Fig. 7D, column 5, lines 63 - 67 and column 6, lines 26 - 57 said leads (e.g., Sn) and said undivided film (e.g., Sn) being formed of the same electrically conductive material.

Regarding claims 21 and 22, these claims merely recite the intended use or the environment in which the semiconductor device of claim 12 is intended to be used. Since the claims fail to define any additional structure, Yoshida et al. anticipates these claims as well.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. in view of Oda (JP-07169795).

Yoshida et al. discloses the claimed invention except for the adhesive being formed of an anisotropic conductive material having conductive particles dispersed in an insulating material. However, Oda teaches the adhesive (108 in Fig. 1) being formed of an anisotropic conductive material having conductive particles dispersed in an insulating material (see Fig. 1 and read abstract). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Yoshida et al. by using the adhesive to be formed of an anisotropic conductive material which is having conductive particles dispersed in an insulating material as taught by Oda. The ordinary artisan would have been motivated to modify Yoshida et al. in the manner described above for at least the purpose of increasing heat dissipation.

6. Claims 3 – 5, 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. in view of Tada et al. '890.

Yoshida et al. discloses the claimed invention except for said leads and said undivided film being formed by etching a conductive foil adhered to said base material of said substrate (claim 3), a conductive foil used when forming said leads is also used to form said undivided film (claim 4), said undivided film being formed simultaneously with said leads (claim 5) and the undivided film being formed to be symmetrical (claims 9 and 18). However, Tada et al. teaches in e.g. Fig. 1, Fig. 18A and column 10, lines 21 – 28 leads (3) and an undivided film (2) being formed by etching a conductive foil (1) adhered to a base material of a substrate (13), a

Art Unit: 2815

conductive foil (1) used when forming said leads is also used to form said undivided film, said undivided film being formed simultaneously with said leads and the undivided film (2) being formed to be symmetrical about a center point of a region in which the semiconductor chip is adhered. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Yoshida et al. by using the conductive foil to form the leads and the undivided film as taught by Tada et al. The ordinary artisan would have been motivated to modify Yoshida et al. in the manner described above for at least the purpose of (1) decreasing manufacturing steps and (2) decreasing dross and spatters (column 2, lines 46 – 62).

Response to Arguments

7. Applicant's arguments, see pages 7 and 8 from applicant's remarks, filed May 28, 2004, with respect to the rejection of claims 1 and 12 under 35 USC § 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art reference.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Paek, Hikita et al., Anderson et al., Ohuchi et al. and Tokuno disclose flip chip semiconductor mounted on a paddle and leads.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

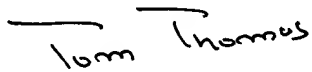
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

c.c.

6/8/04 10:48:20 PM


TOM THOMAS
SUPERVISORY PATENT EXAMINER
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